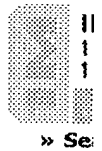




United States Patent and Trademark Office



[Help](#) [FAQ](#) [Terms](#) [IEEE Peer Review](#)

Quick Links

Welcome to IEEE Xplore®

- Home
- What Can I Access?
- Log-out

Your search matched **4** of **1131693** documents.

A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:

You may refine your search by editing the current search expression or enter a new one in the text box.

(area optimal) <and> (technology mapping)

Search

☐ Check to search within this result set

Results Key:

JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 Technology mapping for simultaneous gate and interconnect optimisation

Lü, A.; Stenz, G.; Eisenmann, H.; Johannes, F.M.;

Computers and Digital Techniques, IEE Proceedings- , Volume: 146 , Issue: 1 , Jan. 1999

Pages:21 - 31

[\[Abstract\]](#) [\[PDF Full-Text \(1124 KB\)\]](#) **IEEE JNL**

2 A technology mapper for Xilinx FPGAs

Chikodikar, M.Y.; Laddha, S.; Sirasao, A.:

VLSI Design, 1997. Proceedings., Tenth International Conference on , 4-7 Jan 1997

Pages:57 - 61

[\[Abstract\]](#) [\[PDF Full-Text \(380 KB\)\]](#) **IEEE CNF**

3 A comparing study of technology mapping for FPGA

Martin, H.-G.; Rosenstiel, W.;

Design, Automation and Test in Europe, 1998., Proceedings , 23-26 Feb. 1998
Pages:939 - 940

[\[Abstract\]](#) [\[PDF Full-Text \(16 KB\)\]](#) [IEEE CNE](#)

4 Non-disjoint decomposition of Boolean functions and its application FPGA-oriented technology mapping

Rawski, M.; Jozwiak, L.; Nowicka, M.; Luba, T.;

EUROMICRO 97. 'New Frontiers of Information Technology'. Proceedings of the 23rd EUROMICRO Conference, 1-4 Sept. 1997

Pages:24 - 30


Search


- ☐ By Author
☐ Basic
☐ Advanced
☐ CrossRef

Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

1000

- 
- Access the
-
- IEEE Enterprise
-
- File Cabinet

 **Print Format**

IEEE HOME : SEARCH IEEE : SHOP : WEB ACCOUNT : CONTACT IEEE


[Membership](#) [Publications/Services](#) [Standards](#) [Conferences](#) [Careers/Jobs](#)
IEEE Xplore®
RELEASE 1.5

 Welcome
 United States Patent and Trademark Office


» Se

[Help](#) [FAQ](#) [Terms](#) [IEEE Peer Review](#)
[Quick Links](#)

Welcome to IEEE Xplore®

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

Tables of Contents

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

Search

- ☐ By Author
- ☐ Basic
- ☐ Advanced
- ☐ CrossRef

Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

IEEE Enterprise

- ☐ Access the IEEE Enterprise File Cabinet

Print Format

 Your search matched **4** of **1131693** documents.

 A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.
Refine This Search:

You may refine your search by editing the current search expression or enter a new one in the text box.

☐ Check to search within this result set
Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 Technology mapping for simultaneous gate and interconnect optimisation
Lu, A.; Stenz, G.; Eisenmann, H.; Johannes, F.M.;

Computers and Digital Techniques, IEE Proceedings- , Volume: 146 , Issue: 1 , Jan. 1999

Pages:21 - 31

[\[Abstract\]](#) [\[PDF Full-Text \(1124 KB\)\]](#) **IEE JNL**
2 A technology mapper for Xilinx FPGAs
Chikodikar, M.Y.; Laddha, S.; Sirasao, A.;

VLSI Design, 1997. Proceedings., Tenth International Conference on , 4-7 Jan 1997

Pages:57 - 61

[\[Abstract\]](#) [\[PDF Full-Text \(380 KB\)\]](#) **IEEE CNF**
3 A comparing study of technology mapping for FPGA
Martin, H.-G.; Rosenstiel, W.;

 Design, Automation and Test in Europe, 1998., Proceedings , 23-26 Feb. 1998
 Pages:939 - 940

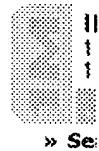
[\[Abstract\]](#) [\[PDF Full-Text \(16 KB\)\]](#) **IEEE CNF**
4 Non-disjoint decomposition of Boolean functions and its application FPGA-oriented technology mapping
Rawski, M.; Jozwiak, L.; Nowicka, M.; Luba, T.;

EUROMICRO 97. 'New Frontiers of Information Technology', Proceedings of the 23rd EUROMICRO Conference , 1-4 Sept. 1997

Pages:24 - 30

IEEE HOME : SEARCH IEEE : SHOP : WEB ACCOUNT : CONTACT IEEE


[Membership](#) [Publications/Services](#) [Standards](#) [Conferences](#) [Careers/Jobs](#)
IEEE Xplore®
RELEASE 1.5

 Welcome
 United States Patent and Trademark Office

[Help](#) [FAQ](#) [Terms](#) [IEEE Peer Review](#)
[Quick Links](#)

Welcome to IEEE Xplore®

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

Tables of Contents

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

Search

- ☐ By Author
- ☐ Basic
- ☐ Advanced
- ☐ CrossRef

Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

IEEE Xplore

- ☐ Access the IEEE Enterprise File Cabinet

Print Format

 Your search matched **4** of **1131693** documents.

 A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:

You may refine your search by editing the current search expression or enter a new one in the text box.

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 Structural gate decomposition for depth-optimal technology mapping LUT-based FPGA design
Cong, J.; Yean-Yow Hwang;

Design Automation Conference Proceedings 1996, 33rd , 3-7 June 1996

Pages:726 - 729

[\[Abstract\]](#)
[\[PDF Full-Text \(388 KB\)\]](#)
IEEE CNF
2 On area/depth trade-off in LUT-based FPGA technology mapping
Cong, J.; Yuzheng Ding;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 2 , Issue: 2 , June 1994

Pages:137 - 148

[\[Abstract\]](#)
[\[PDF Full-Text \(1072 KB\)\]](#)
IEEE JNL
3 DAOmap: a depth-optimal area optimization mapping algorithm for designs
Chen, D.; Cong, J.;

Computer Aided Design, 2004. ICCAD-2004. IEEE/ACM International Conference on , 7-11 Nov. 2004

Pages:752 - 759

[\[Abstract\]](#)
[\[PDF Full-Text \(908 KB\)\]](#)
IEEE CNF
4 Hermes: LUT FPGA technology mapping algorithm for area minimization with optimum depth
Teslenko, M.; Dubrova, E.;

Computer Aided Design, 2004. ICCAD-2004. IEEE/ACM International Conference on , 7-11 Nov. 2004